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Attorney's Docket No.: 10559-202002  
P8465D - ADI APD1632-2-US  
Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Bradley C. Aldrich, et al.      Art Unit: 2183  
Serial No.: 10/828,913      Examiner:  
Filed : April 20, 2004  
Assignee : Intel Corporation  
Title : DSP EXECUTION UNIT FOR EFFICIENT ALTERNATE MODES OF  
OPERATION

**Mail Stop Amendment**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information  
Disclosure Statement and documents listed on form PTO-1449.

This filing is being made before the receipt of a first  
Office action on the merits. No fee is required.

Each enclosed document listed on the herewith Form PTO-1449  
was cited in the parent application, U.S. application serial no.  
09/541,116, filed March 31, 2000. Copies of the prior art are  
not included. Also, enclosed are copies of the International

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being  
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Jennifer H. Payne

Typed or Printed Name of Person Signing Certificate

Applicant : Bradley C. Aldrich, et al.  
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Search Report (6 pages), Written Opinion (8 pages), and  
International Preliminary Examination Report (11 pages) issued  
in the related International Patent Application.

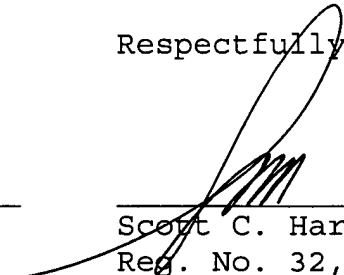
The documents are in the English language; hence no concise  
explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the  
return of a copy of the enclosed form PTO-1449 with the  
Examiner's initials in the left column per MPEP 609 are  
earnestly solicited along with an early action on the merits.

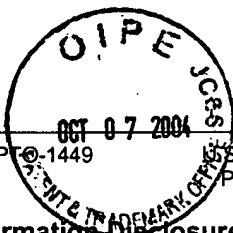
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Respectfully submitted,

Date: 10/1/04

  
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Substitute Form PTO-1449 (Modified)  <b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-202002	Application No. 10/828,913
	Applicant Bradley C. Aldrich, et al.		
	Filing Date April 20, 2004	Group Art Unit 2183	

**U.S. Patent Documents**

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	4,748,585	05/1988	Chiarulli, et al.			
	AB	5,432,728	07/1995	Curtet			
	AC	5,517,436	05/1996	Andreas, et al.			
	AD	5,666,169	09/1997	Ohki, et al.			
	AE	5,717,923	02/1998	Dedrick			
	AF	5,933,797	08/1999	Håakansson, et al.			
	AG	6,092,094	07/2000	Ireton			
	AH	6,370,630	04/2002	Mizuyabu, et al.			
	AI	6,418,527	07/2002	Rozenshein, et al.			
	AJ						
	AK						

**Foreign Patent Documents or Published Foreign Patent Applications**

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL	0 654 733	05/1995	Europe				
	AM	WO 98/32071	07/1998	WIPO				
	AN	WO 99/31601	06/1999	WIPO				
	AO							
	AP							

**Other Documents (include Author, Title, Date, and Place of Publication)**

Examiner Initial	Desig. ID	Document
	AQ	Bermak, et al., "High-density 16/8/4-bit configurable multiplier", <i>IEE Proc.-Circuits Devices Syst.</i> , 144(5):272-276, (1997).
	AR	Kim, et al., "4-way Superscalar DSP Processor for Audio Codec Applications", Proceedings of the 1998 IEEE International Conference on Acoustics, Speech and Signal Processing, ICASSP, '98, Seattle, WA, USA, May 12-15, 1998, IEEE International Conference on Acoustics, Speech and Signal Processing, New York, NY, Vol. 5, Conf. 23, May 12, 1998, pp. 3117-3120.
	AS	Singh, et al., "GaAs Low-Power Integrated Circuits for a High-Speed Digital Signal Processor", <i>IEEE Transactions on Electron Devices</i> , 36(2):240-249, (1989).

Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	